Custom Design of an Analogue Input Digital Output Interface Card for Small Size PLCs

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Abstract: This paper describes the design and implementation of an interface card (IC) with analogue input and digital output, designed for use with small size PLCs, which do not support interface features. The absence of generic I/O interface modules due to the differences in PLCs design and software, validates the importance of such work. The IC costs about one third of an analogue I/O dedicated proprietary module. The IC was utilized in a closed loop temperature control system. The results of the work are satisfactory.

Keywords: Interface card, PLC program, PWM, ADC, analogue input digital output card.

INTRODUCTION

The subject of this paper is a custom design of an analogue input digital output PLC interface card. Nowadays many PLC manufacturers offer for extra cost analogue I/O interface modules dedicated for their PLCs. The design of generic interface modules is still not common. This is due to the differences in PLC's structures and software. This work is an attempt in the said direction. This, also, helps in solving the problem of controlling a heater temperature by using custom designed PID/PWM program [1]. The card input is not programmable and the card does not include a coprocessor. All logic, math, data move and other operations are carried out by the PLC control processing unit (CPU). This interface card is intended to be used with small PLCs, which do not support analogue input interface (AII). The interface card (IC) is designed for one analogue input, but it could be expanded to accommodate multi analogue inputs by utilizing an 8-channel multiplexer existing in the (ADC) chip.

Very often, when it is required to control final power elements, switch-mode amplifiers [2] or (D) type amplifiers [3] are utilized. This is due to their high efficiency when compared with linear power amplifiers [4]. In order to function, power switches of switch-mode amplifiers are controlled by using PWM signals. The generation of PWM signal is supposed to be done by a PLC subroutine which is driven by the output of a PID/PLC program [1]. This decreases the total cost of the control system, since there is no special hardware for the generation of the PWM signal, also it gives flexibility for modifying the control strategy from

another point of view, as such there is no need for a (DAC) and power amplifier in order to control the final power element.

PRACTICAL DESIGN CONSIDERATIONS

The simplest things are the most powerful. Realizing this fact, an effort has been made to select standard common components with minimal complexity and lowest cost. In order to achieve the target the following requirements have to be met.

- Taking into account that the voltage signal range at the transducer output is different from the required voltage range at the ADC input, zero and span circuits [5] are used for signal level matching between the transducer and (ADC). This same approach was applied in order to match signals levels between the PLC output and the power switch trigger unit.
- In order to input process variable signal to the PLC, an (ADC) with adequate resolution is utilized to convert the analogue signal to a digital one.
- The heater and the PLC are located beside each other. So there is no need for serial signal transmission between the (ADC) and the PLC. Thus through isolating optocouplers, an eight bit word is transmitted from the (ADC) to the PLC inputs.
- Some kind of timing is needed to drive the ADC, so, the 555 IC timer was utilized. In addition to that, power supply and voltage regulation are required to supply the components of the (IC). To meet this demand the voltage regulator 7805 IC was used.

Building on the above the I/O terminals of the interface card shall be as shown in figure No (1).

The detailed schematic diagram is illustrated in figure No (2). Hereunder is a detailed technical discussion about the interface card components and the selection of their parameters.

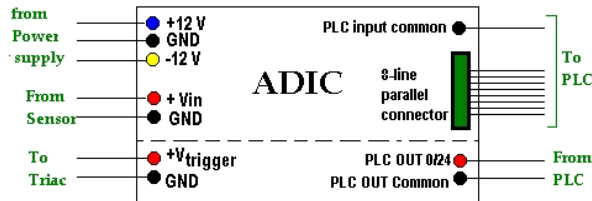Table No (1) contains the specifications of the PLC I/O points.

Fig. 1: I/O Interface card terminals

Table 1: PLC Input Connections

Input number		Input point
0	→	I 1.0
1	→	I 0.1
2	→	I 0.2
3	→	I 0.3
4	→	I 0.4
5	→	I 0.5
6	→	I 0.6
7	→	I 0.7

Output type: Sourcing Transistor
Voltage Range : 20.4-28.8 VDC
Maximum load current: 0-40°C 55°C
Per single point: 0.75A 0.50A
Per 2 Adjacent points   : 1.00A 0.75A
All points Total : 4.00A 3.00A
Leakage current: 100 µA
Switching delay: 25 µS ON, 120 µS OFF

Plc I/O Rating And Connections: Figure 3 shows PLC I/O connections. The PLC type is Siemens Simatic S7-200 with a 214 CPU. The version of the PLC is DC/DC/DC, and this means that it has a DC power supply, and also DC inputs and outputs.

The CPU 214 DC/DC/DC accepts 20.4 to 28.8 as a power supply voltage range, consuming 85 mA typically for the CPU, and 900 mA on maximum load. It is fused with a 1 A, 125 V, slow-blow fuse.

Technical Specifications Of Interface Card Components
Zero and Span Circuit: The output of a transducer rarely matches the levels needed to be provided to the controller. Although it is possible to get high-level

signal using different conditioning techniques [6], we still have inconvenient voltage range to deliver to the (ADC). In the used experimental temperature control board [7] the transducer gives 100 mV/ºC. This means that 2 to 8 volts result from applying 20 ºC to 80ºC to the transducer. Unfortunately the ADC accepts 0 to 5 volts as the analogue input. This issue is frequently encountered and therefore must have a standard solution. The solution is to implement zero and span circuit which is shown in figure No (4).

Two inverting amplifiers (LM741CN) are used in this circuit. The voltage at the circuit output e_{u2} is equal to:

$$e_{u2} = +\frac{R_f}{R_i}e_{in} + \frac{R_f}{r_{os}}V \qquad (1)$$

The above equation is the equation of a straight line: y = mx + b where, y is the dependant variable, x is the independent variable, m is the slope (gain or span) and b is the intercept (offset or zero).

$$m = \frac{R_f}{R_i} \quad and \quad b = \frac{R_f}{R_{os}}V.$$

Understanding the above analogy we can define components parameters.

$$m = \frac{V_{out(max)} - V_{out(min)}}{V_{in(max)} - V_{in(min)}};$$

Thus $\frac{5V - 0V}{8V - 2V} = \frac{5}{6} = 0.83$

Considering that $m = \frac{R_f}{R_i}, R_f$ is selected to be relatively large so that R_i will be large enough to avoid loading the transducer.

Selecting R_f = 82.5 kΩ gives

$$R_i = \frac{6}{5} \times 82.5 = 99 \text{ kΩ}$$

In order to enable adjustment of the gain, R_i is selected as a fixed resister with a resistance 49.5 kΩ and series 100 kΩ potentiometer. This facilitates the variation of m in a relatively wide range (0.55-1.67).

In order to get the offset, it is recommended to substitute the obtained values into the circuit equation at one point.

$V_{out} = m V_{in} + b \qquad ; \quad at \qquad V_{in} = 2 \text{ V}$

and $\qquad V_{out} = 0 \text{ V} \quad ;$

o V = (5/6)(2 V + b) ; b = -1.6 V
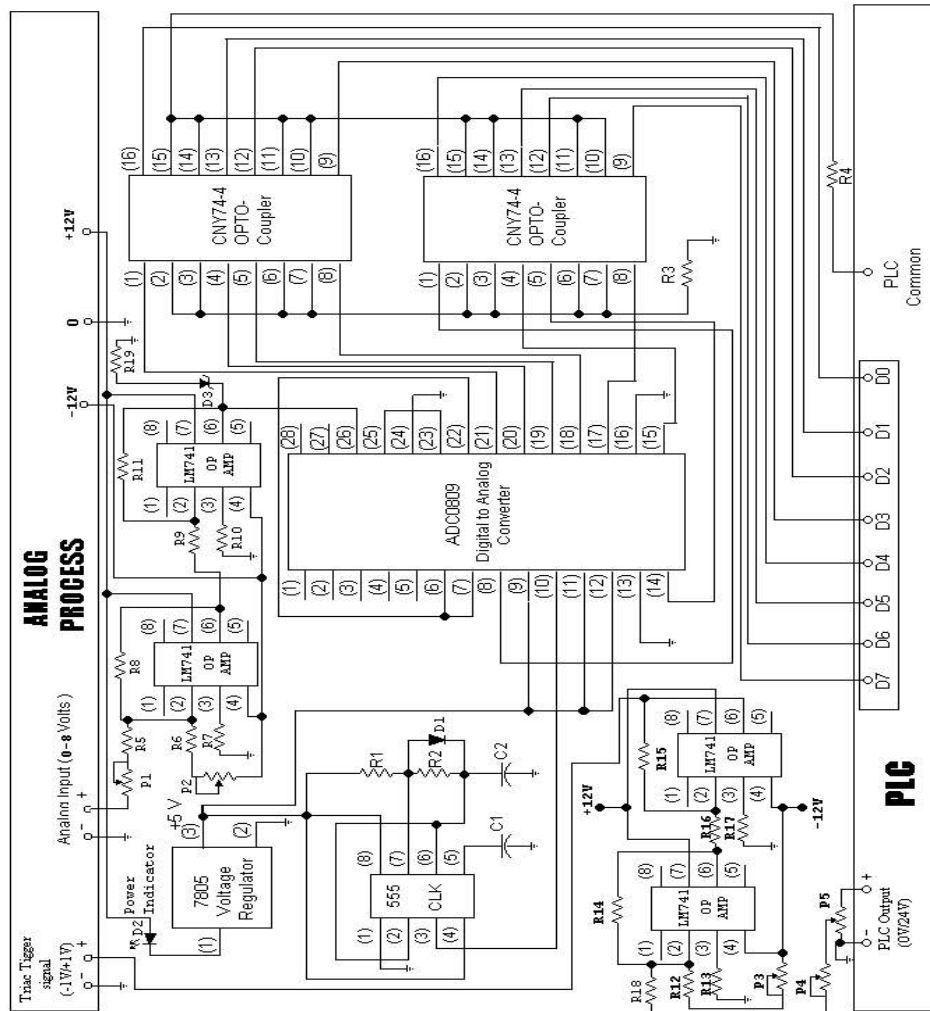
R1	750Ω	R7	1.2 kΩ	R13	39 kΩ	R19	75 Ω	C1	0.1µF
R2	750Ω	R8	100kΩ	R14	47 kΩ	P1	100 kΩ	C2	100µF
R3	75 Ω	R9	2.2 kΩ	R15	2.2 kΩ	P2	500 kΩ	D1	Silicon
R4	15 Ω	R10	1.2 kΩ	R16	2.2 kΩ	P3	1 MΩ	D2	2.2V LED
R5	120 kΩ	R11	2.2 kΩ	R17	1.2 kΩ	P4	300 kΩ	D3	Zener 5V
R6	325 kΩ	R12	325kΩ	R18	150 kΩ	P5	2.4 kΩ	--	--

Fig. 2: ADIC Schematic

To meet the need negative offset, we selected V = -12 as the negative power supply voltage.

$$R_{os} = \frac{R_f V}{b} = \frac{82.5k\Omega(-12)}{-1.6V} = 594k\Omega$$

Therefore, R_{os} was selected as a 220 kΩ fixed resistor with a series 500 kΩ potentiometer. This permits to vary (b) within the range (-1.375 to -4.5) V.

The above implies that

$$R_{comp} = R_f // R_i // R_{os} = 41.83k\Omega$$

Checking the other specified point we find:

V_{out} = (82.5 kΩ / 99 kΩ) * 8 V + (82.5 kΩ / 594kΩ) * -12 V = 5 V

Analogue to digital converter (ADC): An 8-bit resolution is appropriate for temperature measurement and control. Therefore ADC 0809 CMOS IC was selected .
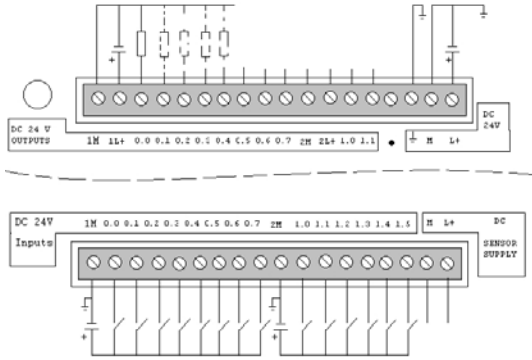
Fig. 3: PLC Input and Output Connections

Input type :   Type 1 Sinking
ON State Range   :15-30 VDC, 4mA minimum
35VDC, 500 ms surge
 ON State nominal   : 24 VDC, 7 mA
OFF state maximum   : 5VDC, 1mA
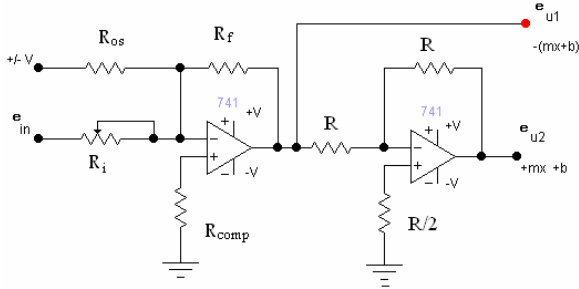Optical Isolation   : 500VAC, 1 Minute

Fig. 4: Zero and Span Circuit

Table 2: Practical ADC0809 Digital Output

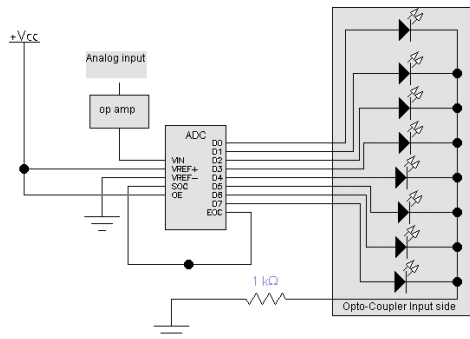| Analog input [Volt]	Binary output
4.90	11111111
4.00	11001101
3.02	10011001
2.25	01110011
1.00	00110100

Fig 5: ADC is Completely Isolated
SOC: Start of Conversion, OE: Output Enable, EOC: End of Conversion
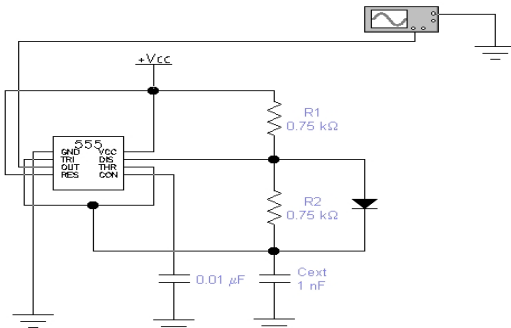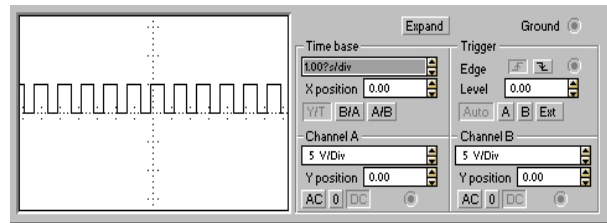

Fig. 6:555 Timer in the Astable Mode
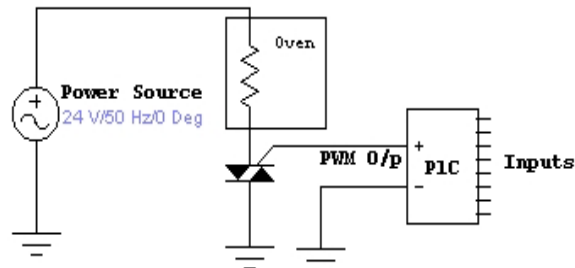

Fig 7: 555 I/O Output (640 KHz, 50% Duty cycle)
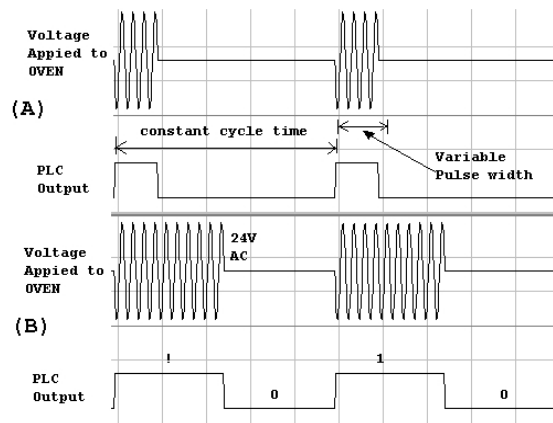

Fig 8: simplified output power circuit

Fig. 9: Triac Response to PLC PWM signal

(a) 20% Pulse width
(b) 50% Pulse width

This is a data acquisition component, monolithic CMOS device with 8-channel multiplexer and microprocessor compatible control logic. Detailed specifications are shown in the National Semiconductor Corporation Catalog.

This IC is fully isolated from the PLC by using optocouplers as shown in figure No (5). ADC resolution is 0.01961 V.

Experimentally, the ADC was mounted on the test board, also different analogue voltages were applied to the (INO) pin, and the digital outputs were observed. Table No (2) shows some of the conversion results.

TIMER 555 IC: The timer 555 IC is used to generate a 640 KHz, 50% duty cycle, 5 volts pulse train to drive the ADC0809. To achieve this timer, IC was connected to operate in the astable mode as astable vibrator as shown in figure No (6).

The frequency of oscillation is calculated by using equation:

$$f_r = \frac{1.44}{(R_1 + 2R_2)C_{ext}} \qquad (2)$$

And the duty cycle is equal to:

$$\frac{R_1}{R_1 + R_2} \times 100\% \qquad (3)$$

For f_r = 640 KHz, duty cycle = 50%, C_{ext} = 1nF, solving the last two equations simultaneously gives: $R_1 = R_2 = 750\Omega$.

The timer circuit in figure No (6) was simulated using the EWB software and the circuit output was scoped as shows in figure No (7).

Optocoupler: The duel and quad optocoupler ICs 74-4 / 74-2 use single transistor output stages in which the base terminal is not externally available. The CNY 74-4 / CNY 74-2 implemented digital interfacing between the CMOS IC (with TTL level output), and also the PLC 24 volts input circuit. Applying a 5 volt pulse signal to the led terminals causes the phototransistor to conduct 24 volts to the high voltage circuit (PLC input circuit). Temic Semiconductors shows detailed description, ratings and switching characteristics.

Power Supply: Referring to the ADC0809 datasheets we notice that the V_{cc} may take values from 4.5 VDC to 6 VDC, while the reference voltage must be stabilized at 5 volts in order to obtain optimum functionality and accuracy. Luckily, the 555 IC can be fed with a wide range of V_{cc} DC voltages including 5V (giving a 5V amplitude clock acceptable by ADC0809). This leads to underline the need of a 5V voltage regulator. The 7805

IC implements this function accompanied by adequate heat sink. It can provide 1A with fixed 5 volts between V_{out} and GND.

Output Power Circuit: After adequate conditioning, the 0/24 VDC output of the PLC is used to trigger the triac as shown in figure No (8).

Average power delivered to the load depends on pulse width. Figure No (9) illustrates this.

CONCLUSIONS

- For using PLC program as a controller in a closed loop system, a custom design analogue input digital output interface card was designed, assembled and tested.

- As an interface card is three times cheaper than standard propriety analogue I/O model, the designed interface card could be utilized with PLCs which do not support analogue input interface.

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