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Design of a Low Power and High Speed Comparator using MUX based Full Adder Cell for Mobile Communications

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Abstract: This paper presents an implementation of comparator (1-bit) circuit using a MUX-6T based adder cell. MUX-6T full adder cell is designed with a combination of multiplexing control input and Boolean identities. The proposed comparator design features higher computing speed and lower energy consumption due to the efficient MUX-6T adder cell. The design adopts multiplexing technique with control input to alleviate the threshold voltage loss problem which is commonly encountered in Pass Transistor Logic (PTL) design. The proposed design successfully embeds the buffering circuit in the full adder design which helps the cell to operate at lower supply voltage compared with the other related existing designs. It also enhances the speed of the cascaded operation significantly while maintaining the performance edge in energy consumption. In the proposed design, the transistor count is minimized. For performance comparison, the proposed MUX-6T comparator (1-bit) is compared with four existing full adders based comparators using BSIM4 model parameters. The simulations are performed for 65nm process models indicate that the proposed design has lowest energy consumption along with the performance edge in both speed and energy consumption. The variants namely area and power of the proposed comparator is also compared with the published author designs to validate its suitability for low power and high speed mobile communication applications.

Keywords: Comparator, Full Adder Cell, Multiplexor, PTL, CMOS, High-Speed, High-Voltage, Low-Power

Introduction

Comparators are widely used in electronic circuits after operational amplifiers. They are also mostly popular as 1-bit analog-to digital converters. Analog to digital conversion efficiency mainly depends on the input sampling process. Comparator determines the digital equivalence of the analog signal with the help of its sampled input. In today's world, portable battery operating devices are growing rapidly due to the low power methodologies predominance in high speed applications. Power minimisation can be attained by inching towards feature size reduction techniques (Etienne and Sonia, 2007a). The Short Circuit Channel (SCE) effect due to feature size reduction introduces various non-idealities and other process variations that affect the entire performance of the device. In analog-to-digital converters low noise margin, low power dissipation, low hysteresis, less offset voltage and high speed is essential for portable and mobile communication devices. The design of comparators with low power consumption, low offset along with the high speed forms the major interest in research today to achieve overall higher performance of ADCs. In the past, pipeline and flash based ADC architectures implement comparator based pre-amplifier designs. Offset voltage becomes a major constraint in pre-amplifier based comparators. Dynamic comparators are an alternative to overcome this problem to make a comparison during every clock cycle and need much low offset voltage. However, the power consumption is very high in dynamic comparators in comparison with the pre-amplifier based comparators. The major drawback of these dynamic comparators is the fluctuating output signal from the latch stage during clock transitions. This is due to the noise occurrence at the input terminals. The proposed converter design using multiplexer based full adder cell topology eliminates the noise at the input and reduces the power consumption and delay.

Comparator is the fundamental and performs a predominant role in the arithmetic unit of digital systems and there are numerous topologies available in the design of CMOS comparators with different operating speed, noise margin, complexity and its power dissipation. In this study comparator design implementation is done by full adder which is the basic functional blocks of the digital VLSI circuits. Several enhancements in approaches have been rendered related to its structure since its invention even one can implement the comparator by flattening the logic function directly too. The main concern of such refinements is to reduce the transistors count which intern increase the speed of operation and minimize the power consumption. One of the major advantages in reducing the transistor count is to increase the fabrication density of a single chip thereby reducing the total chip area (Etienne, 2009).

In digital system arithmetic, magnitude comparators are used for comparison. Magnitude comparator is a combinational circuit which compares two binary numbers for e.g., A and B and then their relative magnitude is determined and outcome is specified by three states which indicate whether A<B, A=B and A>B shown in Fig. 1. This research work focuses on designing a high speed and low power magnitude comparator (1-bit) using MUX based full adder cell. The magnitude comparator with two inputs namely A and B consist of full adder, inverters at one of the input and AND gates at the output. The threes outputs are for various combinations of its inputs and its truth table as shown in Table 1.

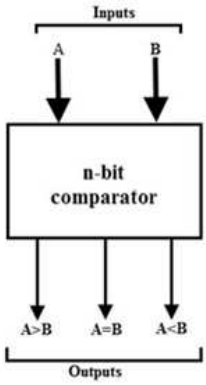

Fig. 1. Block diagram of a comparator

Table 1. Truth table of 1-bit comparator

Inputs		Outputs		
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Review of Comparator Design

Many researchers in the recent past aim to focus on numerous approaches towards CMOS comparator design implementations using various logic styles that were incorporated in formulating a uniform method of design. In CMOS comparator design power consumption, speed and circuit area become the major criteria of concern. However, the design methodology constraint in CMOS forms a major bottleneck scenario in the circuit design of comparators. To overcome this each individual parameter performance criteria are analysed, estimated, along with their behavior to build-up both qualitative and quantitative apprehension of numerous designs were presented in the literature. Different comparator (1-bit) designs have been introduced by researchers using conventional CMOS, PTL, GDI, TG and hybrid logic styles. Comparator (1-bit) design using conventional CMOS consisted of 42 transistors, PTL comparator design consisted of 18 transistors, GDI comparator design consisted of 16 transistors, TG comparator design consisted of 36 transistors and hybrid comparator design consisted of 17 transistors.

Comparator forms a fundamental functional unit of an Arithmetic and Logic Unit (ALU) in ASIC's and Digital Signal Processors (DSPs) used in mobile communication applications. Various concepts in CMOS comparator design with the help of numerous design logic methods were presented by researchers in the literature. Power consumption, speed and chip area are the three major estimates in predicting the overall performance of a CMOS comparator design (Etienne and Sonia, 2007b). However, these estimates conflict with one another i.e., each individual estimate can't be optimised independently (Anjali *et al*., 2013). Hybrid comparator (1-bit) design consisting of 17T by using GDI and PTL logics was introduced. The design of comparator (1-bit) consisted of 8 PMOS and 9 NMOS. The hybrid comparator (1-bit) design was based on 9T full adder cell. PTL and GDI logic was implemented in the design of the full adder module. Full adder cell was used as the basic building block in the design. The hybrid logic used in the design of full adder suffers from switching delay and thereby causing additional propagation delay along with switching penalty. The design performance was evaluated by simulating BSIM-3 and BSIM-4 models. Hybrid PTL and GDI logic used in the design introduced additional complexity in the circuit there by degrading the overall performance.

Hassan and Mehra (2015) considered three different approaches in the design of CMOS comparator (1-bit). The focus was on auto-generated, semi-custom and full-custom based layout designs. Auto generated approach is easy to design but takes more area and consumes less power than semi-custom design approach. Semi-custom design takes less area but consumes much more power than auto generated design. Finally, full-custom design

takes less area and consumes less power than both auto generated and semicustom design. Full-custom design is more efficient in terms of chip area and power consumption when compared with auto generated design and semi-custom design. The work didn't highlight on comparator's performance as the approach was mainly restricted to different types of layout generation.

Comparator (1-bit) design using four 10T GDI full adder cells was implemented by Anjali and Pranshu (2014). GDI full adder cell, XOR-XNOR cell included 6 transistors. GDI XOR-XNOR output is used to generate the carry and sum of the full adder cell. The comparator (4-bit) consisted of 28 NMOS and 28 PMOS which is less when compared with the other comparator (4-bit) designs using CMOS, PTL and TG logic. The comparator (4-bit) consisted of four full adder cells designed by using GDI logic. Two hexadecimal inputs were used to generate two 4-bit binary outputs. In cascade four AND gates were used to generate A=B output of the comparator (4-bit). Output sum of first full adder acted as one of the input to the first AND gate. Output carry of first GDI Full adder acted as a C_{in} input of the succeeding full adder. Output carry of last full adder acted as B>A output of the comparator (4-bit). The GDI logic introduces power overhead due to more number of PMOS transistors used in the design and need restoration logic to improve the performance in cascade.

Comparator (2-bit) design was introduced by Rachana *et al*. (2016) using hybrid full adder module. The design included 16 transistors. The design was validated by comparing it with the conventional CCMOS, CPL, TGA and TFA based adder modules by using Tanner EDA Tools 13.0. TG and CMOS combination was used in the hybrid logic design of full adder. Sum and carry signals were generated using XNOR modules. The XNOR module consumed more power in the adder design. In order to compare two numbers in digital systems, magnitude comparators were used. The hybrid logic used in the full adder design introduces additional propagation delay along with need of higher switching activity.

Aggarwal and Kaur (2015) introduced magnitude comparator (2-bit) design by using CMOS, PTL and GDI logic. CMOS based comparator (2-bit) consisted of 88 transistors to provide three outputs i.e., A>b, A>B, A=B. PTL logic consisted of 28 transistors which are relatively less in numbers compared to the conventional CMOS. The GDI based design used three inputs: G i.e., gate which is common to NMOS and PMOS, P i.e., input to the source/drain of PMOS and N i.e., input to the source/drain of NMOS. The GDI cell consisted of only two transistors. GDI based comparator consisted of 30 transistors. Four XOR gates, two MUX and two AND gates were used in the design of full adder. The inverter at the input of XOR produces XNOR by using 3 transistors. The inverter used to produce XNOR consumes more area and high power consumption thereby degrading the design performance.

Proposed Comparator Design

MUX Full Adder

Proposed comparator (1-bit) is implemented using MUX-6T based full adder introduced by Ramana Murthy *et al*. (2012) consumes lower power than other logic styles described in the literature. The architecture of the proposed comparator is shown in Fig. 2. It consists of 6 transistors. Most of the existing adder design techniques have been considered along with its pros and cons in all the previous studies conducted (Ramana Murthy *et al*., 2014). The proposed adder is based on simplified Boolean identities along with multiplexing control technique with less number of transistors. The Boolean expressions for sum and carry of adder (1-bit) with 3-inputs A, B and C are given by expressions shown in Equations 1 and 2 respectively:

$$SUM = \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C} + A\overline{BC} \quad (1)$$

$$CARRY = AB + AC + BC \quad (2)$$

Schematic Diagram

To obtain the three comparative outputs inverted input at the B input terminal is given to the full adder design and C input is connected to the ground. Carry output directly act as A>B output of the comparator (1-bit). For the A=B and B>A, different input combinations of AND gate has been used. For generation of B>A input combination for the AND gate is B and A1 and for the generation of A=B input combinations for AND gate is SUM and V_{DD} as shown in Fig. 3.

The proposed comparator (1-bit) is implemented using MUX-6T full adder circuit and contains only 22 transistors. The architecture of the proposed comparator is shown in Fig. 4.

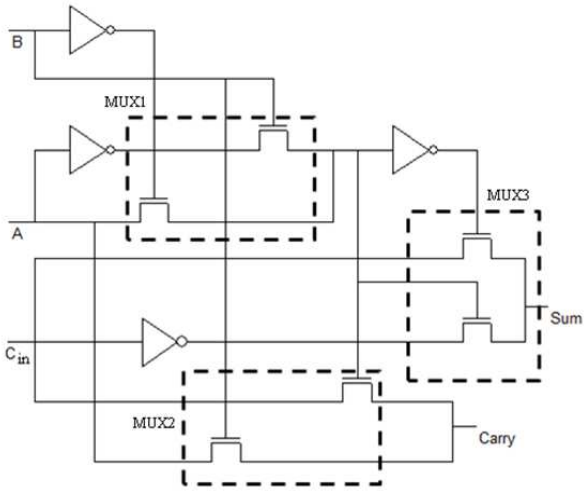

Fig. 2. MUX 6T full adder

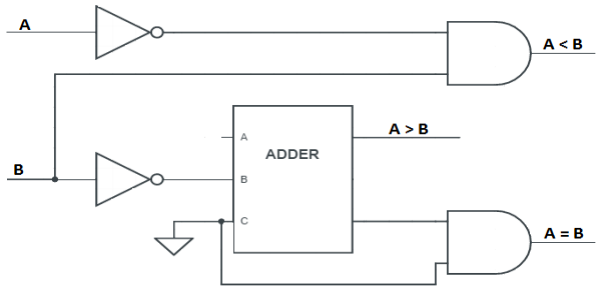

Fig. 3. Full adder based comparator block diagram

Results and Discussion

The four-different comparator (1-bit) circuits namely Shannon, MUX-14T, MCIT-7T, MUX-12T and the proposed MUX-6T comparator are designed by using pass-transistor logic using DSCH3.5 CAD tool at schematic level and layout are generated by Microwind 3.5 layout editor. Fig. 5 shows the layout of the proposed comparator which is simulated at 65 nm feature size using BSIM 4 VLSI CAD tools environment. The Shannon theorem adder based comparator proposed by Senthilpari *et al*. (2009) gives voltage swing restoration. Due to this problem, the Shannon comparator circuit consumes high power and operates at low speed. The MUX-14T adder cell based comparator circuit introduced by Senthilpari *et al*. (2010) was designed by using multiplexer concept which has few complex nodes in the design. The input node drivability consumes high power to transmit the voltage level. The MCIT-7T adder cell based comparator circuit proposed by Senthilpari *et al*. (2011) was designed by multiplexing control input technique. The input nodes transient consumes additional power thereby leads to high power consumption. The MUX-12T adder cell based comparator circuit introduced by Ramana Murthy *et al*. (2011) was designed by multiplexing control input technique. The carry circuit has buffering restoration unit at A⊕B and its complement results in high power dissipation and propagation delay. The MUX-6T adder cell based comparator circuit gives low power dissipation, high speed and less occupying area compared to previous adder cell based comparator circuits as shown in Table 2. The multiplexing design concept reduces leakage current due to less transistor count and switching event in the transistors.

The MUX-6T comparator circuit is compared with the other comparators at 120, 90 and 45 nm feature sizes. The transient analog simulation of the MUX-6T comparator is shown in Fig. 6. The MUX-6T comparator shows its superiority over the other published comparator circuits in terms of power and surface area as given in Table 3. The better performance of the MUX-6T comparator is mainly due to high tasked flow of current, absence of swing restoration, less transistor count, high transition activity in NMOS transistors and low critical path in comparator circuit.

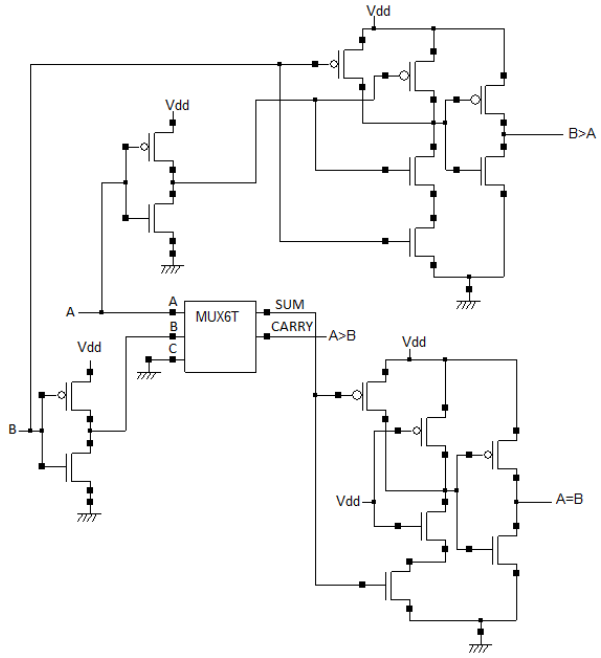

Fig. 4. MUX 6T comparator

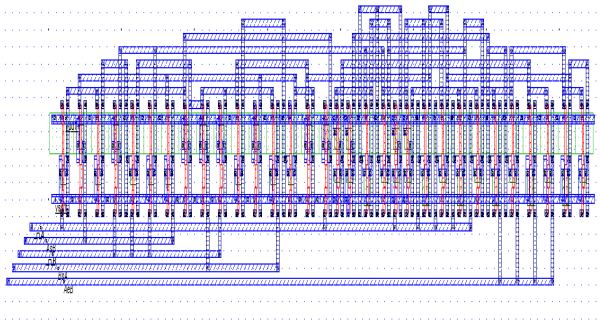

Fig. 5. Layout diagram of the MUX 6T Comparator

Power Dissipation

Power dissipation in a digital circuit can be mainly categorised into two components: One is dynamic dissipation that occurs due to the presence transient current during switching activity, discharging and charging of load capacitances and second is static dissipation that occurs due to the leakage current or other current continuously drawn from the power supply. The static power dissipation is the product of supply voltage and the leakage current. Power dissipation in the pass transistor logic is moderately high due to the presence of dynamic power dissipation in NMOS transistors. Power consumption mostly depends on the switching activity of the logic gates, which in turn depends on the inputs received on the comparator circuit. Power analysis can be estimated for a set of vectors by using a simulator and by evaluating the total capacitance switched during each clock transition at every transistor's node.

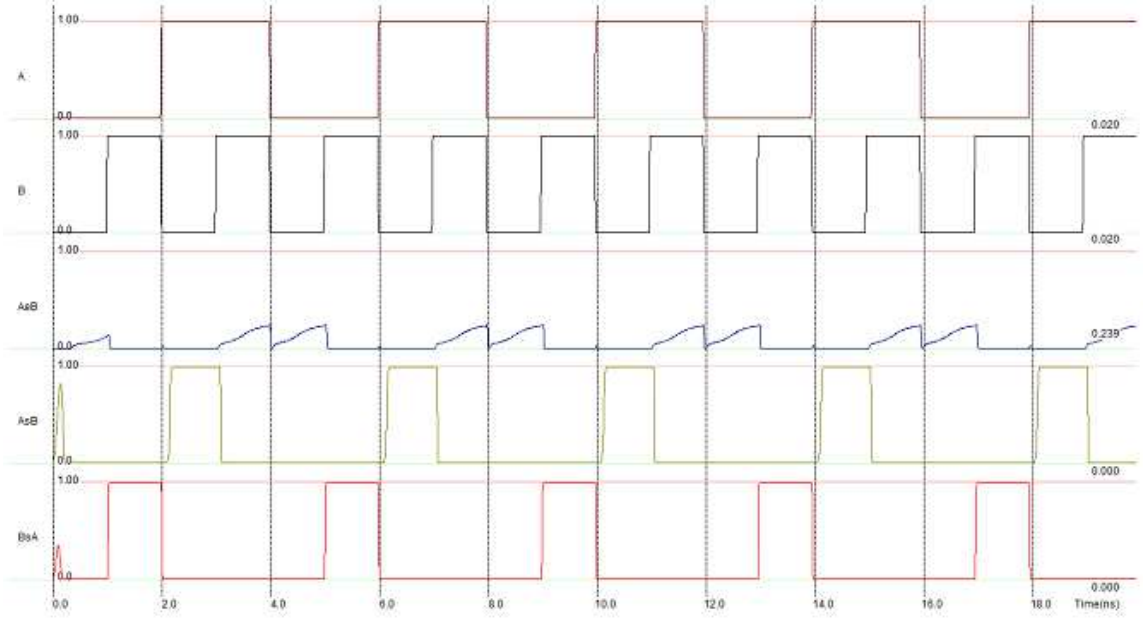

Fig. 6. Transient simulation of the MUX 6T comparator

Table 2. Comparison of the proposed MUX 6T comparator (1-bit) power dissipation, propagation delay and area with MUX 12T, MUX 14T, MCIT 7T and Shannon based comparators

Type	Power supply	65nm	90nm	130nm	180nm
Proposed comparator	Power (µW)	29.46	34.36	75.82	97.68
	Delay (ps)	6	8	9	12
	Area (μm^2)	22×7	23×10	30×10	68×21
1-bit comparator (MUX 12T)	Power (µW)	46.33	51.33	84.87	130.33
	Delay (ps)	7	7	10	14
	Area (μm^2)	29×7	32×12	45×11	74×51
1-bit comparator (MUX 14T)	Power (µW)	46.55	98.5	119.06	182.22
	Delay (ps)	15	17	24	32
	Area (μm^2)	29×9	38×12	54×11	114×24
1-bit comparator (MCIT 7T)	Power (µW)	42.23	51.66	78.11	139.82
	Delay (ps)	15	16	21	26
	Area (μm^2)	25×8	29×10	50×10	79×55
1-bit comparator (Shannon)	Power (µW)	112.27	250.6	428.26	720.56
	Delay (ps)	15	19	24	35
	Area (μm^2)	47×7	54×11	60×13	124×23

Table 3. Comparison of proposed MUX 6T comparator (1-bit) area, power dissipation, propagation delay and PDP with other published author results

Comparator type	Feature size	Area (μm^2)	Reduction %	Power (µWatt)	Reduction %	Delay (ps)	Reduction %	PDP (fJ)	Reduction %
1-bit comparator (MUX 6T)	65nm	154		29.46		6		0.176	
proposed comparator	90nm	230		34.36		8		0.274	
	130nm	300		75.82		9		0.682	
	180nm	1428		97.68		12		1.172	
Direct logic based comparator (Chandrahash and Veena, 2014)	120nm	326.2	8.03	9.341	-87.68				
4-bit comparator design (TG) (Anjali and Pranshu, 2014)	120nm	1320.3	77.27	-					
1-bit Hybrid comparator (Anjali *et al*., 2013)	120nm	329.3	8.89	-					
Hybrid 2-bit comparator (Rachana *et al*., 2016)	90nm	-	-	7458	99.5			1336	99.9
PTL logic comparator (Aggarwal and Kaur, 2015)	45nm	140	-	-					
	90nm	296.7	22.48	-					

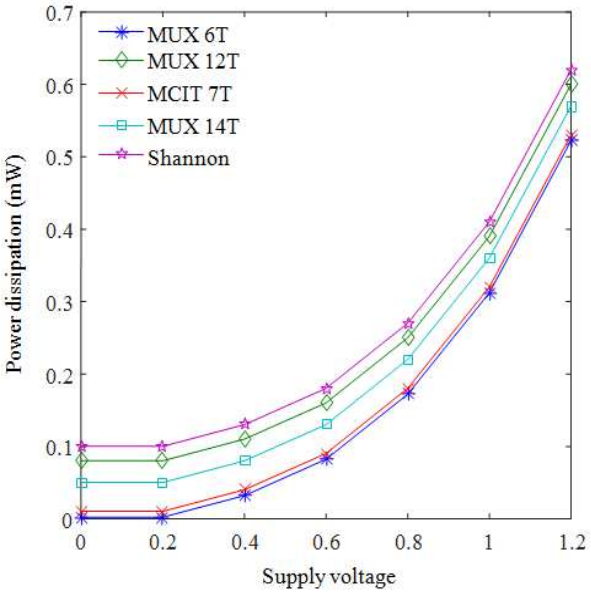

Fig. 7. Voltage Vs. power dissipation

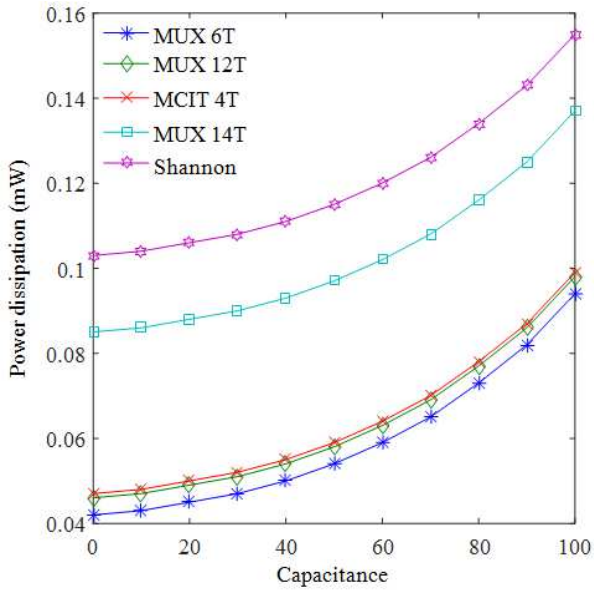

Fig. 8. Capacitance Vs. power dissipation

In MUX 6T comparator (1-bit) the current flow of the carriers is regulated. The gate capacitance is also important for dynamic power consumption as shown in Equation 3:

$$P_{dynamic} = \frac{V_{DD}}{T}\left[Tf_{sw}CV_{DD}\right] = CV_{DD}{}^{2}f_{sw} \quad (3)$$

The effective gate capacitance for power is typically somewhat higher than for delay. This is caused by the delay in switching the drain with the source (or) vice-versa. Hence, C_{gd} is effectively doubled. The effective capacitance for dynamic power consumption is shown in Equation 4:

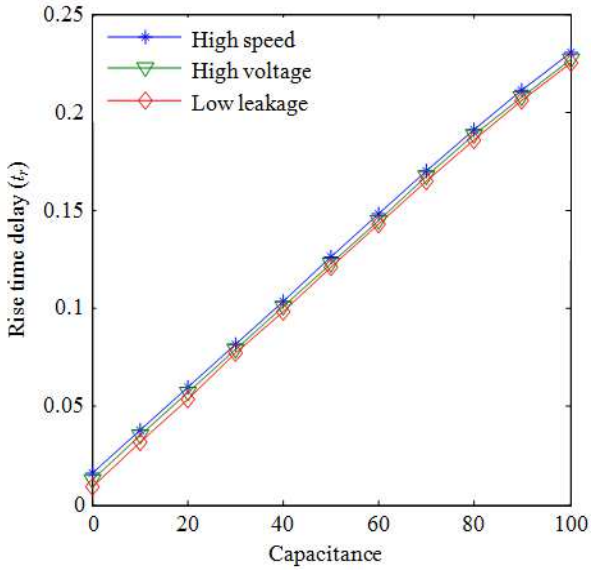

Fig. 9. Rise time delay of MUX-6T comparator

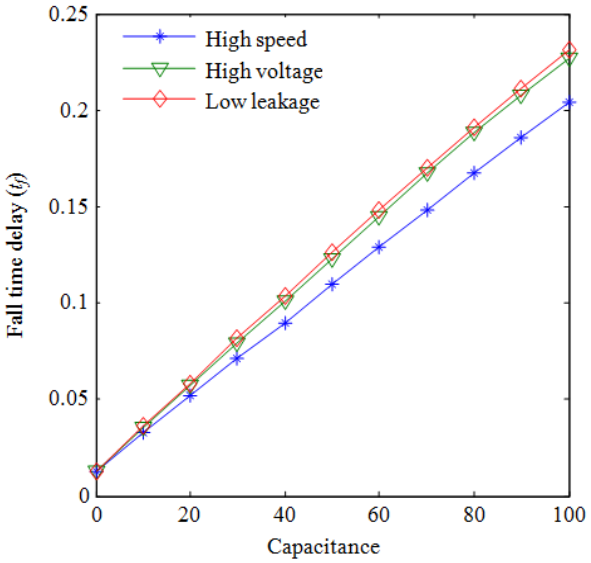

Fig. 10. Fall time delay of MUX-6T comparator

$$C_{eff-power} = \frac{\int i_{in}(t)dt}{V_{DD}} \quad (4)$$

This capacitance can be divided by the total transistor width to find the effective capacitance per micron. The MUX-6T comparator is designed with the regular arrangement of transistors which results in low critical path and finally it leads to low power dissipation compared to the other comparators. The power dissipation of the proposed comparator by varying input supply voltage and load capacitance in comparison with other designs is shown in Fig. 7 and 8 respectively.

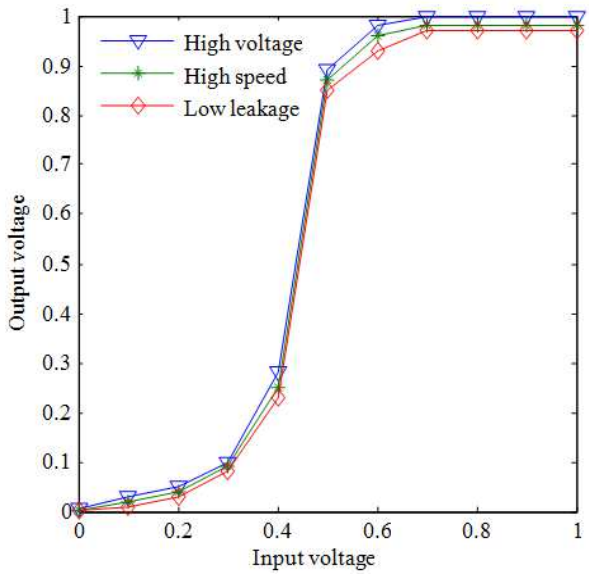

Fig. 11. Static characteristics of MUX-6T comparator

Propagation Delay

When a logic gate input signal is changed, there involves a propagation delay prior to the change in the logic gate output. This is mainly due to output node load capacitance effect. The comparator (1-bit) circuit is designed by considering the latest trends in the high-speed circuits. The MUX-6T comparator design is simulated to evaluate the propagation delay by considering the Low-Power (LP), High-Speed (HS) and High-Voltage (HV) NMOS and PMOS transistors. The rise time and fall time delay response of the proposed comparator is shown in Fig. 9 and 10 respectively. The HS NMOS and PMOS cells based design shows a better performance in terms of propagation delay compared to other cell FETs. Even though the exact analysis of the circuit propagation delay in digital design is quite complex, a simple first-order derivation shown in Equation 5 can be used to show its dependency of the comparator circuit parameters. W/L ratio for a HS FET cells is low when compared to the HV and LP FET cells which in turn produces least propagation delay as shown in Equation 5:

$$T_d = \frac{C_L V_{DD}}{I} = \frac{C_L V_{DD}}{\eta (W/L)(V_{DD} - V_{th})^2} \quad (5)$$

T_d is the propagation delay of the comparator, η is a technology-dependent constant, W and L are respectively the transistor width and length and Vt_h is its threshold voltage. The absence of glitching and the reduced switching activity in MUX-6T comparator design minimizes the propagation delay there by it is more suitable for high speed mobile communications.

The static characteristics of the proposed comparator (1-bit) correspond to the variation plot of the output voltage versus the input voltage. The simulation involves a step-by-step increase of input voltage and the monitoring of output voltage levels. In the case of a comparator this characteristic can be observed for all the three output voltage levels which indicate whether A<B, A=B and A>B. The performance of the static characteristics for the proposed comparator is evaluated by considering HV, HS and LP PMOS and NMOS cells as shown in Fig. 11.

Conclusion

In this study, a MUX-6T adder cell based comparator (1-bit) has been proposed. The MUX-6T comparator (1-bit) along with four other existing adder cell based comparators is designed by using DSCH 3.5 and the layouts are generated by using Microwind 3.5 CAD tool. The MUX 6-T comparator (1-bit) is compared with the previous researcher's designs at 120, 90 and 45nm feature sizes. The MUX-6T comparator (1-bit) shows better performance in terms of area, power and PDP. The rise time and fall time delay response of the MUX-6T comparator (1-bit) is analysed by using HS, HV and LP NMOS and PMOS transistors by using BSIM 4 tools. The transient simulation of the MUX-6T comparator (1-bit) is performed to validate the design. The static characteristics of the MUX-6T comparator (1-bit) is also analysed by using HS, HV and LP NMOS and PMOS transistors. Furthermore, the MUX-6T comparator (1-bit) is compared to the four existing adders based comparator simulated values for power, propagation delay, PDP and area. The simulation results show better performance than the other four existing full adder based comparator circuits. This shows that the MUX-6T comparator (1-bit) may be suitable to use at low power and high speed mobile communication applications.

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Author's Contributions

G. Ramana Murthy: Initiated the idea of this research and was involved in the planning, design and implementation of this study. He conducted some literature research as well.

Ajay Kumar Singh: Involved in the constructive approach in the design, analyses and write-up of this study. He was also involved in a lot of the literature review compilation and methodology.

P. Velraj Kumar: Participated in the organization of ideas, interpretation of the results and participated in conducting and analyzing the results and contributed to writing of the manuscript.

Tan Wee Xin Wilson: Involved in the design and implementation of this project. He conducted the analysis and simulation of the project.

Ethics

This article is original and contains unpublished material. The corresponding author confirms that all the other authors have read and approved the manuscript.

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