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High Performance and Low Leakage 3DSOI Fin-FET SRAM

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Abstract: In recent semiconductor designs, the major key factors: Competent device simulations, precise device characterization, well power optimization, new architectural design and cost-effective fabrication drives the designers attention towards multi gate transistors as an alternative to MOSFET. Non planner device structures are a competitive edge over planner devices. Silicon-on-Insulator (SOI) FinFETs are hopeful among variety of multi-gate structures as they have simple fabrication, Superior gate control, lower subthreshold leakage and minimized susceptibility to process variations. Low leakage memory cells play a significant role of power consumption in the recent VLSI Systems. In this study, Ultra-low Voltage Asymmetric Short Gate (UVASG) FinFET is modeled with TCAD tools for low leakages and FinFET based SRAM has been proposed as a substitute for the bulk devices.

Keywords: Non Planner Devices, SOI, Ultra Low Voltage, FINFET, TCAD, SRAM

Introduction

According to the ITRS-2014, 94% chip area is occupied by the semiconductor memories. Aggressive scaling results in two ways. Cell miniaturization through device modeling, the peripherals and interconnects scaling. Device scaling to nanoscale regime produces many problems and sensitive to process variation (http://www.radioelectronics.com/info/data/semicond/fet-field-effect transistor /finfet- technology-basics.php).

Progress of bulk CMOS scaling includes short-channel effects, sub-threshold leakage, gate-dielectric leakage and device-to-device variations (http://www.itrs2.net/itrs-reports.html). Reverse Bias leakage, Subthreshold Leakage, Gate Oxide Tunneling, Gate-Induced Drain Leakage and Punch-through effects are some of effects (Ijjada and Rao, 2013). Subthreshold and Gate Oxide leakages are more with the device shrinking. Up to 65 nm, subthreshold leakage dominates the gate leakage. Beyond 65 nm the scenario has been reversed. For a new technology, 18% gate oxide thickness (tox) is reducing. The minimum thickness for reliable operation is 2 nm but at 65 nm it is 1.4 nm. Hence the gate leakage is 1000 times more than subthreshold leakage (Ijjada *et al*., 2011). No Efficient technique for controlling gate oxide leakage alternatively high k materials can do better. Now the single largest leakage component is subthreshold leakage. Short channel effects in bulk MOSFET increase body doping concentration consequently carrier mobility and tunneling effects increases the off-state currents. To have a control over DIBL effect, high halo doping preferred but it degrades on current and increases BTB Tunneling. To utilize the scaling benefits with minimum SCEs the device structures are continuously trying to modify. FinFET results due to the relentless increase in levels of integration. Based on the earlier Depleted Lean-channel Transistor design (Wu *et al*., 2006), FinFET is built on an SOI substrate making it a non-planar and double gate device (Mil'shtein *et al*., 2012). Double gate FINFETs overcomes scaling hurdles and its significant feature of FinFETs is that the front and back gates can be made independent and biased to manage the current and threshold voltage (Colinge, 2008). Typical FinFET is shown in the Fig. 1.

$$Effective\ gate\ length, L_{eff} = L_{gate} + 2L_{ext} \quad (1)$$

$$Effective\ gate\ Width, W_{fin} = T_{SI} + 2H_{fin} \quad (2)$$

$$Channel\ Width = n_{fin} * H_{fin} \quad (3)$$

where, 'L_{gate}' is poly length, L_{eff} is effective gate length, n is the number of fins more fins are preferred

to achieve good control over the device performance. Distance between the top gate and buried oxide is the fin height (H_{fin}), silicon fin thickness (T_{SI}) is the distance between back and front gate oxides, Tox is the oxide thickness, *Lg* is the gate length, *Wg* is the width of the source to drain. Gates are made independent to have separate control over the back and front gates. Back gate allows flexibility in the design and offers new biasing schemes to enhance the device speed and reduce the off current. A small back gate reverse bias reduces 90% of off current and 60% of on current (Muttreja *et al*., 2007).

FinFET has near ideal sub-threshold behavior, which is nearly impossible with planar technology (Ijjada and Sudha, 2016). Fin height, thickness and gate length are the critical parameters. Fin thickness determines the effective channel length. Top gate oxide thickness is much greater than sidewall oxide thickness. To restrict the electron motion in particular path chooses Lgate/4 < Tsi. Heavy doping causes short channel effects and dopant fluctuations (Manju and Senthil Kumar, 2015). Gate leakage, mobility of carrier and device reliability can be improved with reduced body biasing as below:

$$L_{eff} = L_{gate} - \Delta L \tag{4}$$

$$C_{g\_F} = C_{o\_Fin} WL \tag{5}$$

$$C_{g\_F} = C_{o\_Fin} WL \tag{6}$$

where, C_{g_F} is gate capacitance, *L* and *W* are the length and width of the channel, C_{o_F} is the gate capacitance per unit area and *D* is the gate oxide thickness. For 45 nm technology the parameters are in Table 1.

FinFET works in four different modes, namely, Low Power (LP) mode, tied-gate (SG) mode, Independent Gate (IG) mode and LP/IG mode. In IG mode FinFET, the opposite sides of gates are restrained independently. The number of transistors is reduced by providing the multi-threshold voltage by independent gate biasing. With minimization of leakages, there is an unprecedented improvement in cell's stability and performance. The interference in read cycle is experienced due to direct-data-access mechanism which can be minimized without increasing the size of a transistor. Hence, the better stability in SRAM cell is achieved by IG-FinFET.

Table 1. 45 nm technology parameters

	Tox (nm)	Vdd (V)	Vth (V)	C_Fin (fF)	L_mean (µm)	W-Mean (µm)
NMOS	0.9	1	0.3423	2.5	0.45	1.5* L_mean
PMOS	0.92	1	-0.231	-	-	-

SRAM Design

Subthreshold regime scaling of MOSFET requires heavy channel doping to control the SCEs and super hallow implants to control sub surface leakage currents. Heavy doping degrades mobility due to impurity spreading and a high transverse electric field in the on state worsens sub-threshold swing and increases parasitic junction capacitance. Thus, for a given off-state leakage current specification, on-state drive current is ruined. Off-state leakage current is improved due to band-to band tunneling between the body and drain (Guo *et al*., 2011).

Conventional CMOS 6T SRAM cell is shown in the Fig. 2 and is simulated a 45 nm technology the results are shown in the chapter-III.

IV (Current-Voltage) characteristics of n-Fin-FET device are shown in the Fig. 3 as the back gate biasing voltage varies from -0.2 to 0.2 V. In cut- off region, $V_g < V_{th}$, the characteristics are drawn with the help of drain to source current (Ids) is (Raj *et al*., 2011) given by:

$$I_{ds} = qD_n \frac{n_i W_{fin} H_{fin}}{L_{eff}} e^{(V_{gs} - \Delta\varphi_f)/V_T} * \left(1 - e^{-V_{ds}/V_T}\right) \tag{7}$$

$\Delta\phi_f$ = Work function difference
v_T = Volt equivalent temp
n_i = Intrinsic carrier concentration
D_n = Minority carrier diffusion constant

For positive V_{ds}, horizontal electric field is established and is smaller than thin oxide field which gives rise to channel formation. As V_{ds} increases with constant V_{gs}, pinch-off forms depletion region with high electric field and enters into saturation region as shown in Fig 3. The experimental FinFET does not suffer from excessive channel length modulation, due to the superior gate-controllability over the channel region. For V_{ds} = 0.1 to 1.0 V. Drain current does not have linear relation for L = 1 because the parasitic capacitance/resistance affects in addition to the mobility degradation due to the relaxed tensile strain. Channel length modulation effect is not excessive due to the excellent control of gate over the channel. **S**ince gate terminal is electrically isolated from others, the V_{gs} is almost equal to 0. Threshold voltage can be fixed by a metal gate with an apt gate work-function. On the other hand when the fin thickness is diminished below 10 nm, two more components to the threshold voltage have to be considered. The threshold voltage roll-off with channel length for several of oxide thicknesses is given by:

$$V_{th} = \Delta\varphi_f + \frac{kT}{q}\ln\left(\frac{2C_{ox}kT}{q^2 n_i W_{fin}}\right) + \frac{h^2\pi^2}{2qm' T_{si}^{\ 2}} \tag{8}$$

where, *m*' = quantization effective mass. SCEs are minimized successfully without escalating the density of channel doping and gate-oxide thickness scaling; additionally it shows better performance against noise margin. Fin FET based SRAM designs made popular in place of Bulk CMOS SRAM design as Fin FETs having shorter access time and low leakage. Threshold voltage, supply voltage and fin height plays an important role in the leakages minimization. Supply voltage reduction shows strong impact on the SRAM stability. Fin FET based 6T SRAM cell is shown in the Fig. 4.

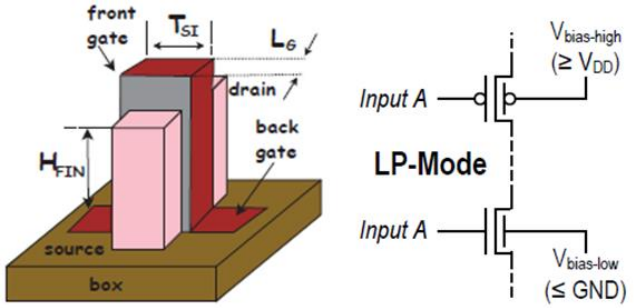

Fig. 1. Typical FinFET device LP mode Fin FET

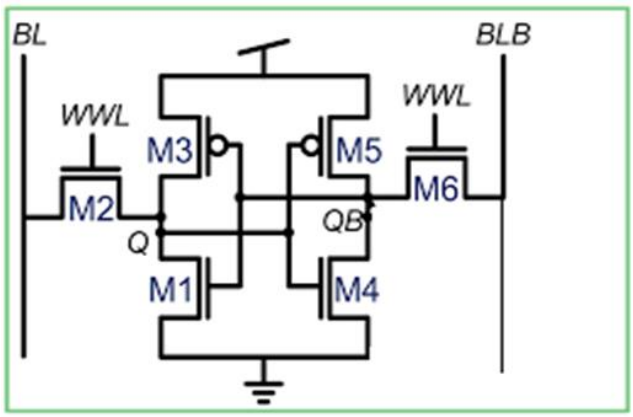

Fig. 2. Conventional 6T CMOS SRAM cell

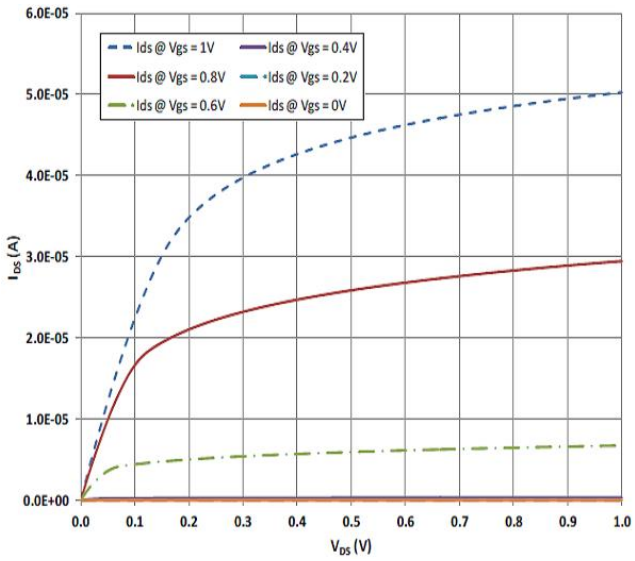

Fig. 3. IV characteristics of nFin-FET with back gate biasing 0.2 V

In Fin FET based 6T SRAM cell, the subthreshold current/power can be calculated by adding subthreshold current in each device in the cell and multiplying with the ½ factor. Assume the symmetric case of SRAM means the half of cell stored ‘‘logic 0’’ and the other half have ‘‘logic-1’’, consider VQ = Vdd and VQB = 0.

Simulation Results

The read cycle of 6T CMOS SRAM cell is shown in the Fig. 5. The waveform depicts the process reading the cell stored value. To read either logic high or logic low value which is already cell’s stored value can be started by connecting WL = Vdd and both the bit-lines are connected to Vdd. If the corresponding node value is logic high then the bit-line is high other words it pulls to ground.

The write cycle for logic low and high are shown in the Fig. 6 and 7. To write logic “0” into the cell, connect bit-line to Vdd and bit-line bar to ground in addition to the WL is pre-charged with Vdd.

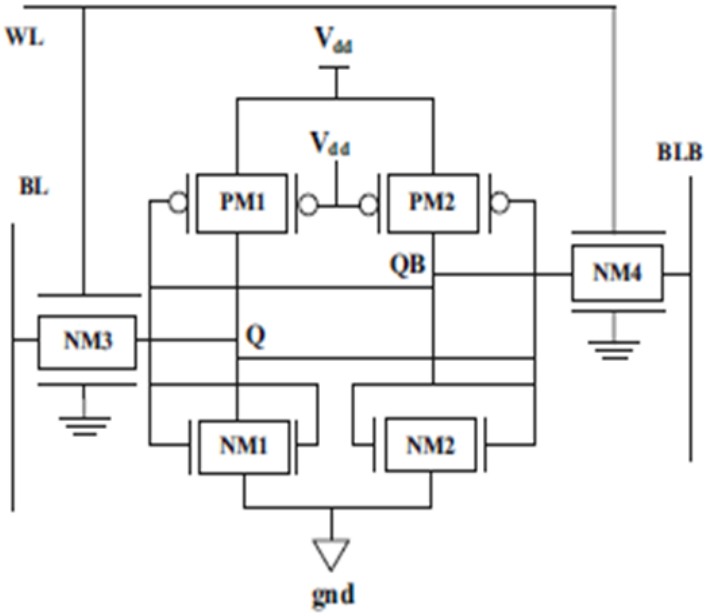

Fig. 4. 3D SOI FinFET based 6T SRAM (Manju and Senthil Kumar, 2015)

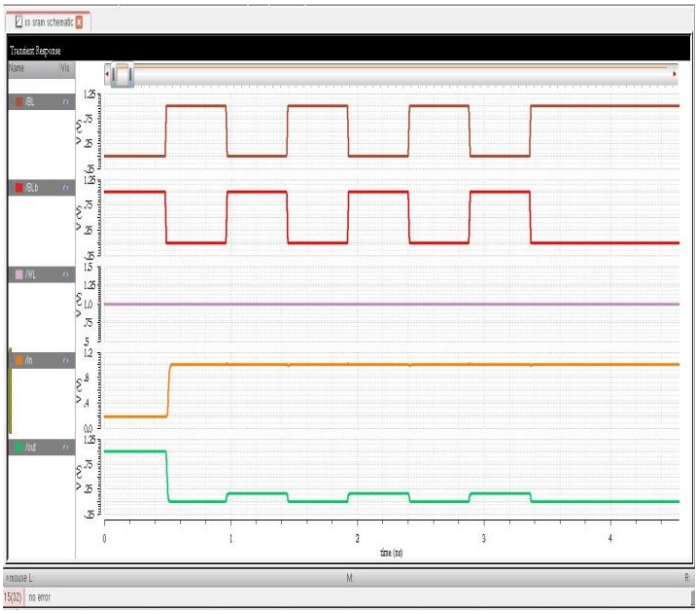

Fig. 5. Read cycle for CMOS SRAM

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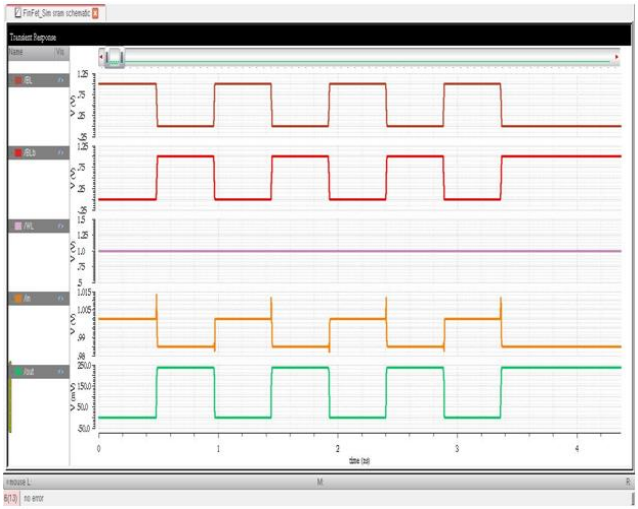

Fig. 6. Write logic-0 simulations

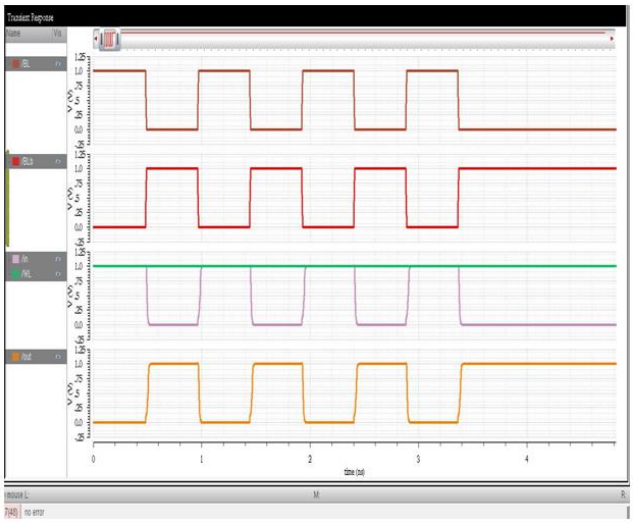

Fig. 7. Write logic-1 simulations

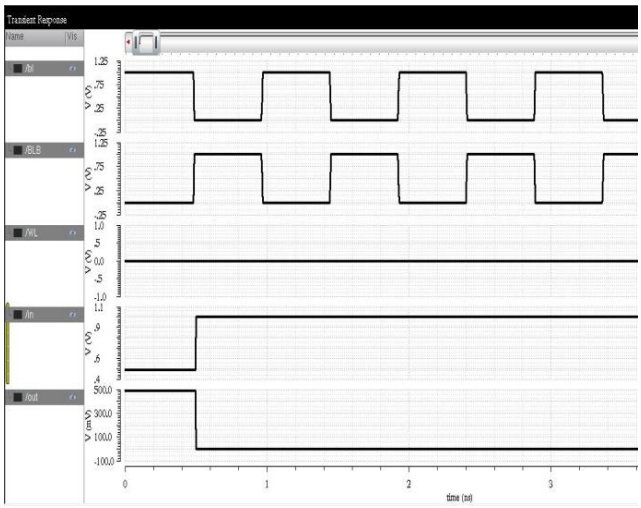

Fig. 8. Read cycle of FINFET SRAM

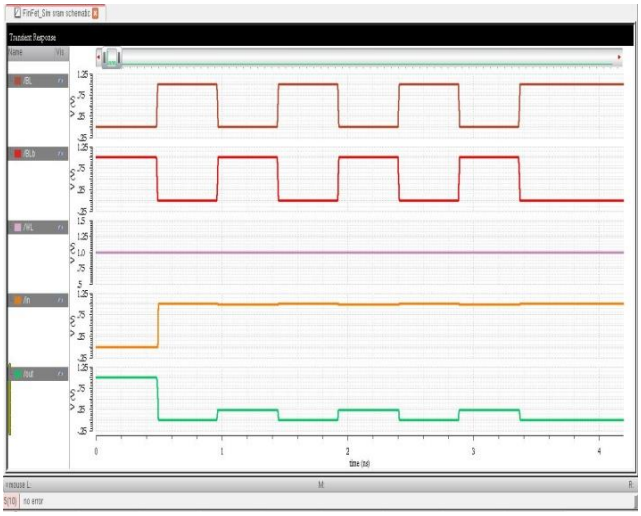

Fig. 9. Write logic-0 FinFET simulations

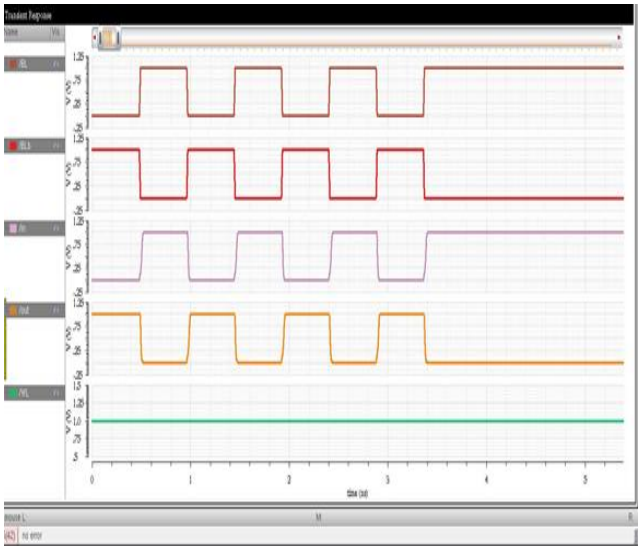

Fig. 10. Write logic-1 FinFET simulations

The simulation waveforms to write logic "1" in to the cell is shown in the Fig. 9. To write logic "1" in to the cell, connect bit-line to ground and bit-line bar to vdd apart from pre-charging WL to vdd. The simulations for the CMOS 6T SRAM cell are performed with 45 nm GPDK files with cadence virtuoso tools.

FinFET 6T SRAM Simulations

The read and write procedures of Fin FET based 6T SRAM are almost similar to the CMOS 6T SRAM cell. FinFET 6T SRAM cell read cycle is shown in the Fig. 8.

Write cycles to write logic "0" and logic "1" into the SRAM cell are shown in the Fig. 9 and 10 respectively.

After observation of read/write cycles of 6T CMOS/FinFET SRAM cells, Fin FET cell shows more stable than CMOS cell.

Result Analysis

Cells have been designed using the Cadence/TCAD, PTM/GPDK files used for the analysis. The performance of each design compared based on stability and power. All the plots indicate the clear domination of FinFET devices over CMOS circuits. From Fig. 6 and 8 it is clear that the stability is more with FinFET. From the Fig. 7 and 9 shows that the overshoots are presented in the CMOS circuits and is due to more parasitics. Based on the results in the Table 2, the variation of stability in both FinFET and CMOS devices are listed.

From the table it is very clear that the FinFET based memories are more stable than CMOS based memories. The optimized FinFET device has low leakages is the main cause for this situation. The peak power/average power of CMOS/FinFET technologies is given in the Table 3.

Table 2. Stability comparison for CMOS/FinFET 6T SRAM cells

	Stability	
Voltages (V)	CMOS cell	FinFET cell
1	Stable	More Stable
0.8	Stable	Stable
0.6	Less Stable	Stable
0.4	Unstable	Stable
0.2	Unstable	Less Stable

Table 3. Power performance comparison

Power	Peak	Average
CMOS	2.58 mW	2.602 mW
FINFET	0.091 mW	0.089 mW

From this, it is clear that FinFET shows better performance in all aspects compared to CMOS designs. In the plots the linear slope indicates the amount of current flowing through the capacitor. As it is a constant slope, this implies that the current through the capacitor is constant. This again proves to be an advantage over MOSFET as it does not violate Absolute Maximum Current Rating and hence reliability increases.

Conclusion and Future Scope

FinFET has been proposed as a promising alternative for bulk CMOS to carry out device scaling. FinFET characteristics are more realistic and efficiently reduce DIBL and parasitic capacitances there by offers better Ion/Ioff characteristics. FinFET offers lower power and high stability over the CMOS. Power requirement of 6T CMOS SRAM is more than FinFET hence FinFET can be used to design large SRAM circuits.

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Author's Contributions

First author put all her efforts in the modelling of FinFET device modelling and design. The second author great experience helps in the fine tuning of the FinFET parameters. The thired author experienced helped a lot in the labaratory.

Ethics

This article is original and contains unpublished material. The corresponding author confirms that all of the other authors have read and approved the manuscript and no ethical issues involved.

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