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Design and Analysis of SRAM Cell for Smart Application

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Abstract: In today's circuit technology, power consumption and savings are key concerns. The driving reasons behind these innovations are portable devices that require high throughput and low power dissipation, such as computers, phones, and Personal Digital Assistants (PDAs). In portable devices, reducing or decreasing IC dissipated power through design optimization is a big problem, and restricted battery lifespan places very severe restrictions on overall power usage. In this study SRAM circuit for smart applications has been investigated using various factors such as write, read, dynamic, static power with voltage and temperature. The power consumption analysis is the most essential criteria for memory design. Because data stability is a critical concern, affecting both the read and write operations. The implemented 9T SRAM in this study is more efficient than the other SRAM in terms of power usage. When compared with the existing SRAM circuits taken for comparison of different parameters, the proposed 9T SRAM, circuit uses less than 28.2% write power, while it uses about the same for read operation. The data retention voltage for both circuits is 0.29 V, which is utilized to store the data in the circuit. The 32 nm Bulk CMOS process technology from PTM files is used for designing and analysis.

Keywords: SRAM, Static, Dynamic, Read, Write, Temperature, Threshold Voltage, Supply Voltage

Introduction

Low power design chips have resulted in a quick and inventive development requirement to restrict power consumption and the rising significance of portable systems in recent years. These improvements are being driven by portable devices that demand high throughput and low power consumption, such as notebook computers, smart devices, mobile phones, IoT applications, and Personal Digital Assistants (PDA). However, in last few years, power dissipation is given proportionate weight to size and speed consideration. Performance, power, efficiency, and reliability are all important factor of a modern memory-based device, and all should be carefully considered when proposing a new design concept (Ahn *et al.*, 2012). Cache memory is utilised in memory devices for quick operation because of its small power consumption and fast response, SRAM is commonly used in cache memory in mainframe computers, microprocessors, and handheld devices. MuraliMohanBabu *et al.* (2021) stated that the memory involves 70 to 80% area of processor that means it takes much more space and affects the performance and power consumption. The SRAM cell has an advantage that it does not require refresh operation periodically until the power is on (Kumar and Ubhi, 2017). Memory cell design concerns are critical for a variety of reasons. In last few years the drastically advancement in design of SRAM cell improves the performance and reliability. Ojha *et al.* (2020) stated that power dissipation and noise margin of SRAM play an important part for the performance improvement for the low power application. To begin, SRAM cell design is critical to ensuring stable and robust SRAM cell functioning. Second, as on-Chip (SoC) storage capacity continues to expand, SRAM fabricators are pushed to boost packing density.

Thus, the SRAM cell should be minimum size and must meet stability, speed, strength and yield parameters. Near smallest cell size or when the size of the cell is minimum, transistors exhibit higher sensitivity with respect to process change.

Science Publications

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Literature Review

This study will explain how the strength of the SRAM cell is managed by the different characteristics during the study of different completed previous work. Liu and Kursun (2008) have designed a 9T SRAM cell to reduce power leakage and increase data stability. As technology advances, it becomes more sophisticated, increasing the amount of factors that must be considered. Mohana chandrika and Siva Kumar (2022) designed the SRAM cell using using reversible logic gates sensible portable gates for smart computer devices. Huang *et al.* (2013) give a novel approach to find the DRV of SRAM memory when changing parameters. Alluri *et al.* (2020) have designed CMOS circuit which gives the better performance in term of power and speed. Takeda *et al.* (2006) designed a sram cell for high speed application which is RSNM (Read static noise margin) free. The two essential requirements are the Static Noise Margin (SNM), which must be within acceptable limits, and the data read operation, which must not be damaging. Grossar *et al.* (2006) introduced new N-curve metrics for SRAM cell writing capabilities and comparisons were made with SNM. The SNM is a significant factor not just during hold state but also during active operation; this is the most severe constraint to SRAM operation. Another strategy for to improve SRAM reliability on low power dissipation for a 9T SRAM memory is near-threshold voltage region, rapid frequency operation, decreased size, and voltage scalability. Sharma and Akashe (2015) proposed a SRAM cell using two power sources connected to the Bit line and the Bit bar line for use in writing and reading operation. Moghaddam *et al.* (2016) presented a 9T SRAM for the sub-threshold area by decreasing the impacts of the DIBL effect and adjusting the body–source voltage correspondingly. Karthika and SivaMangai (2016) showed that 9T SRAM array with bit interleaving architecture consumes low power with good stability compared to the shared wordline architecture using 6T SRAM cell. Anand *et al.* (2014) proposed two different optimization techniques for more reliable and stable 9T SRAM. By using these two techniques namely, Cell Content Body Bias (CCBB) and Dynamic threshold MOS (DTMOS) for sub-threshold region, it is found to have better RSNM at 0.35V, 41.8% bottom read access time, narrower spread in write access and read access time as 8 and 53.01% respectively over conventional 9T cell. Vatajelu *et al.* (2008) proposed a method for 6T cell to evaluate the outcome of decreasing supply voltage to power the SRAM cell. Simulation carried out for 130, 90 and 65 nm CMOS technology, also SNM and impact of process variation is done. It is found that going down from 130 to 90 nm, SNM decrease by 2.8% also it decreases to 3.2% from 90 to 65 nm. This proposed work implies that scaling down of transistors, results in lower noise immunity. Bhavnagarwala *et al.* (2008) suggested a Dynamic biasing approach in a 9kb × 74b PDSOI CMOS array. This is done for a 6T SRAM cell at 65 nm Model file, which gives minimum voltage reductions of more than 0.2V, lowering the minimum voltage to 0.54, 0.38, and 0.50 V for single voltage and 0.50 V for dual voltage. This fluctuation limit lowers leakage by up to 50% at the cost of a 10% -20% increases in area and a performance loss of less than 5%. Lin *et al.* (2008) presented a write bit line balancing strategy for 9T SRAM cells in the sub-micron area to reduce leakage current while saving up to 32% of dissipated power. This study is carried out utilising HSPICE simulation for the 32 nm technology node, which emphasises and demonstrates superior stability and process variability than typical SRAM cells. Calhoun and Chandrakasan (2006) suggested the effect of SNM in the sub-threshold region on transistor sizes, voltage, global and local fluctuation, and temperature. Also, the worst-case scenario for SNM has been completed. For a 6T cell, it is done on 65nm technology. The results reveal that the aforementioned elements have a considerable impact on circuit performance and SNM. Patil and Bhaaskaran (2017) presented a number of structural options to deal with increasing power dissipation. The author employs numerous strategies to address various challenges such as area concerns, stability, power consumption, and increased power dissipation. Swahn and Hassoun (2006) simulated and compared circuit for 32 nm CMOS and 32 nm FinFET; the FinFET circuit outperforms the traditional/standard 6T CMOS circuit. The result demonstrates that adiabatic FinFETs dissipate 3.62 pW of power (3.6 μW for CMOS), but FinFETs with transmission gates dissipate less energy (J) and produce less power (of the order of pW).

The ordinary or basic SRAM cell requires six transistors, signal routing, and switches for two-bit lines, a word line (also known as row address), and two supply rails. Placing the two PMOS transistors in the N-well necessitates a much bigger footprint. Surana and Mekie (2018) proposed a single-ended 6T SRAM cell which approximately 50% less dynamic power compared to a standard 6T SRAM cell with the same bit error rate. To maximize memory chip density and minimise space, SRAM cell size should be kept as small as feasible in order. Seevinck *et al.* (1987) stated the stability of the SRAM cell is another significant

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issue, which is evaluated by the SNM of a cell. Therefore, method to calculate SNM and its effect on various parameters such as DRV, threshold voltages, temperature, read and write margin has been discussed. Zamani *et al.* (2013) has been implemented a memory architecture in 32 nm technology. By changing schematic design, adjusting the Width by length ratio of transistors, using different optimization techniques, the design can be improved in future and the design can be optimized for low power application.

SRAM Organization

Digital memories are classified into three types: cache, FIFO buffers, and scratchpads. These configurations can be produced by utilizing hardwired logic, however hardwired logic is not general purpose and is only suited for a limited number of applications. A hardwired memory system, on the other hand, is unsuitable for a more general-purpose architecture. A flexible memory system is utilized to solve this problem and make the memory system more general purpose. As a result, the memory system's performance and efficiency improve dramatically. Lu *et al*. (2014) proposed a two-port disturb-free 9T SRAM memory circuit for subthreshold performance to enhance the development of writing capability. Commercial FPGAs and reconfigurable computing fabrics contain reconfigurable memory. Local memory is essential for applications such as buffering and data storage on a local level. The local memory is provided by a completely different mechanism in a reconfigurable memory system. Local memory is supplied in reconfigurable memory by employing block RAMs instead of Configurable Logic Blocks (CLBs). The access widths of the block RAMs may be reconfigured such that they can be utilized as FIFOs, CAMs, or logic blocks. Pavlov and Sachdev (2008) shows a SRAM array organization in which row decoder and column decoder decides the memory cell address in array of $M \times N$ matrix in Fig. 1. The SRAM arrays are so organized that multiple data are stored on one line and can be selected simultaneously while in sequential memories only one word can be stored and selected at a time. The block diagram consists of Row decoder which when gated using adequate timing block signal decodes X row address bits and only one of the word lines either WL_0 or WLN_1 is selected. The SRAM memory contains $N \times M$ arrays in which N rows represent word lines and M represents bit lines. If SRAM cell is placed as arrays in a page manner, to select the accessed page then an auxiliary Z-decoder is required. The memory array is at the Centre of the RAM design. SRAM is volatile memory, which means that no periodic clock pulse is desired to keep stored data for an unlimited period/time. But the RAM is a volatile memory i.e. if power is removed then the data is lost. SRAMs may be arranged as either in word-orientation or bit-orientation.

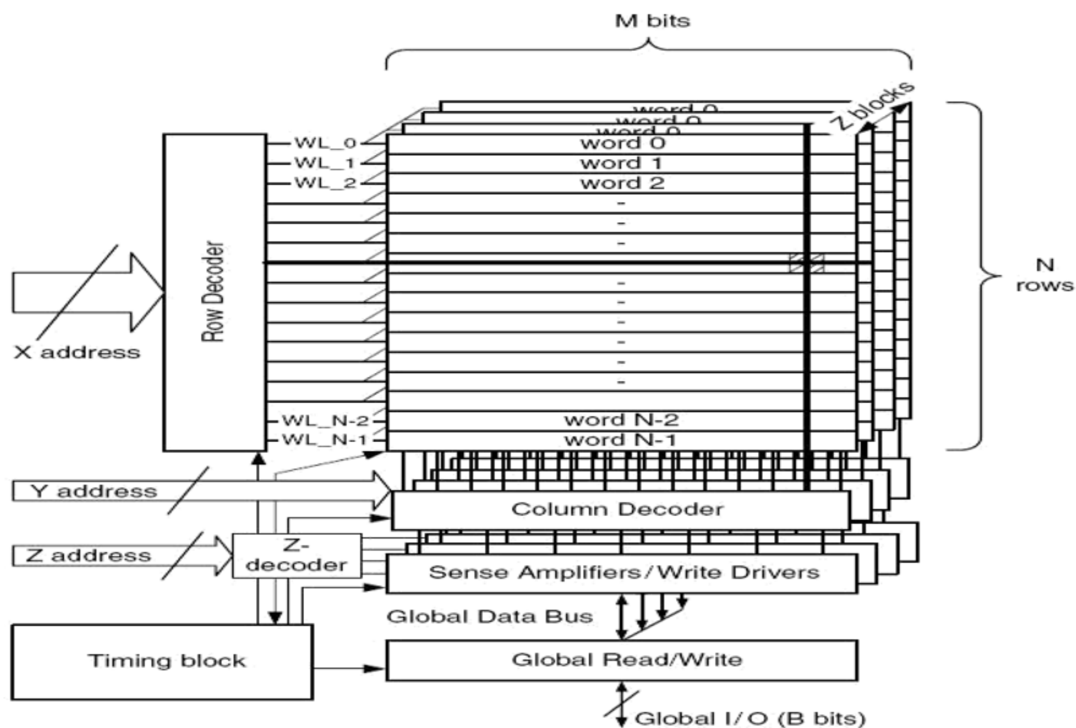

Fig. 1: SRAM Cell array organization

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Materials and Methods

8T SRAM Cell

Anh-Tuan *et al.* (2011), designed a fully differential 8T SRAM memory that enables efficient bit interleaving to achieve soft error tolerance with standard Error Correcting Code. It also consumes less power compared to the standard 6T design. A dynamic column supply voltage is used in this circuit to improve read noise and write capability.

9T SRAM Cell

Tu *et al.* (2012), presented a novel single-ended disturb-free 9T (SEDF9T) SRAM cell memory with the following features: (i) To eliminate Write Half Select (WHS) disturb, a cross-point Write interface with data column based Write WL, (ii) Read buffer to enhance Read stability (iii) common Bit Line (BL) for Read/Write to increase density and bit line power consumption. This 9T SRAM memory consists of a transistor M1-M4 that forms a latch structure and a Read/Write port, M5-M9. In the circuit Word-Line (WL), Virtual VSS (VVSS), Write word line A (WWLA), Write Word Line B (WWLB), and BL are arranged in rows and columns. This single-ended disturb free 9T SRAM is designed using 65 nm technology. Singh *et al.* (2019), proposed a 9T SRAM memory using cadence tool at 45nm technology. This circuit is supposed to be divided into two parts: A sleep transistor connected with standard 6T SRAM memory cell through which the cell is grounded at the bottom available in the left side of the circuit. In this circuit for read operation two transistors are available in the right side. The read and write operation are entirely decoupled and are controlled by separate device within the circuit and the Read Word Line (RWL) decides the read operation.

Proposed 9T SRAM

In this circuit the main aims to assess the applicability of 9T cells for increased performance for low power applications. The SRAM cells in this file are designed for the 32 nm technology node model file. The analysis shows the stability of SRAM cells under the effect of several factors such as threshold (Vth) for PMOS and NMOS, data retention voltage, cell ratio, latency, read power, write power with voltage and temperature changes. All of these parameters impacts are seen for noise margin and the implications of these factors on cell design are investigated.

Figure 2 shows the simplified design of 9T SRAM circuit. This circuit consists of two sub-circuits. The first sub-circuit is basically a standard 6T cell that uses Write Word Line (WWL) to control both access transistors. The data is stored in a latch, formed by two cross connected inverters, which is basically a 6T cell. The second sub-circuit consists of bit line access transistors and a read access transistor. All the implementation and simulation have been carried out for this study in 32 nm technology using tanner tool (version 14.1). The circuit verification and its simulation are carried out using tanner tool.

"Figure 2", shows the schematic of 9T SRAM, represents NMOS_3, NMOS_4, NMOS_5, NMOS_6 and NMOS_7 as access pass transistors. NMOS_7 is having extra Read signal, for performing read operation without any ambiguity at the circuit. "Figure 3" and "4" represents the read operation and write operation respectively.

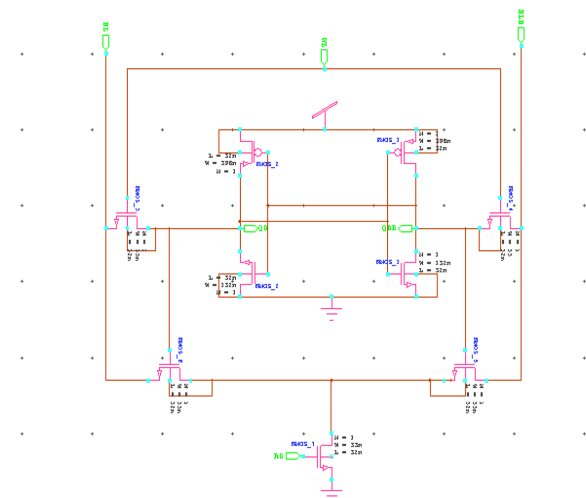

Fig. 2: Proposed 9T SRAM at 32 nm

Read Operation

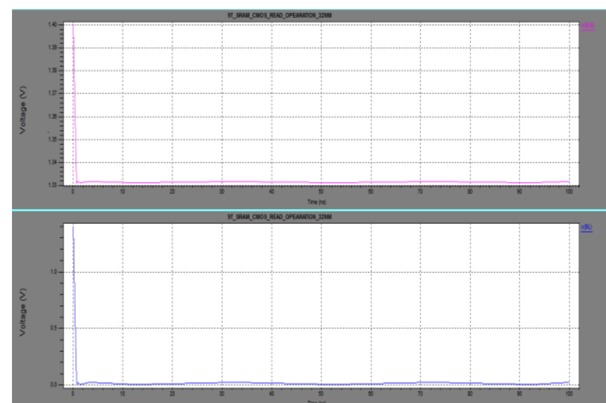

Fig. 3: 9T SRAM read operation

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Write Operation

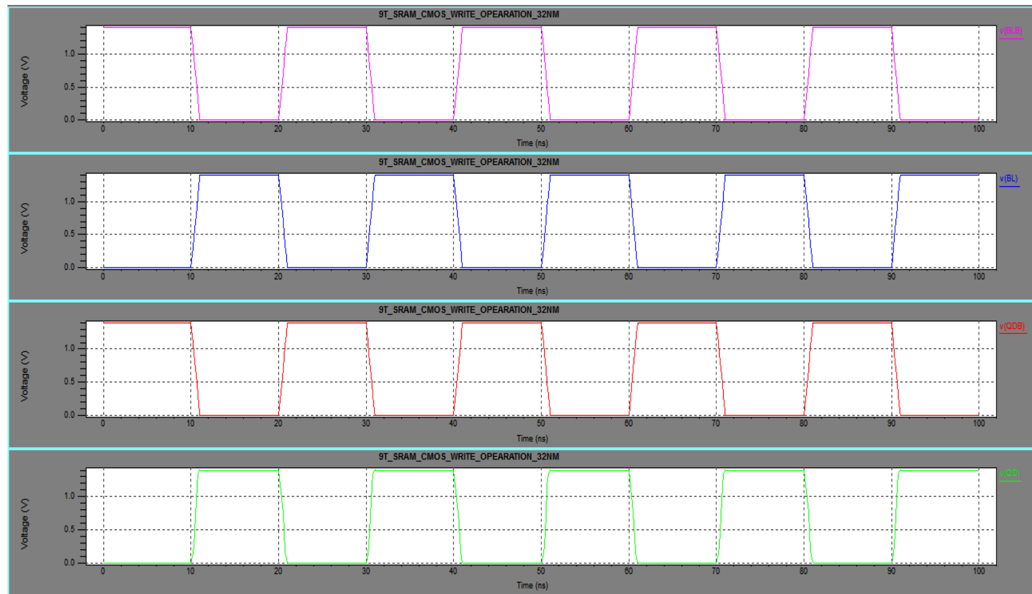

Fig. 4: 9T SRAM Write operation

Results and Discussion

In order to compare and discuss the result of implemented circuit, the work has completed suing the 32 nm predictive technology model. Here the comparison has been made between the different parameter of the implemented circuit with the previously design circuit FD8T (Do Anh-Tuan *et al.*, 2011), SEDF9T (Ming-Hsien Tu *et al.*, 2012) and 9T SRAM (B. Singh *et al.*, 2019).

Power Consumption

For the low power circuit design the key worry is power consumption or the enormous amount of electricity utilized by the circuit. Many approaches, including as dynamic body biasing and word line modulation, are being utilized to improve power usage. Here the BL and BLB are kept equal to half supply voltage, that is the reason this 9T SRAM cells utilize less power than other SRAM cells taken for comparison.

Write and Read Power Versus (V_s) Supply Voltage

A comparison plot of write and read performance versus supply voltage with the existing SRAM cell and the proposed design 9T SRAM cell is shown in “Fig. 5" and "6”. The plot shows that the write power and read power with respect to the supply voltage increases with increased supply voltage.

Static and Dynamic Power Versus Supply Voltage

Static power is dissipated during the inactive state of the circuit whereas dynamic power is utilized during the operating state of the circuit. The variation of this power consumption with supply voltage is shown in “Fig. 7” and “8” compared to SRAM's existing 9T cell at different technology. The static power increases sharply after 1.5 V whereas the dynamic power varies exponentially with supply voltage.

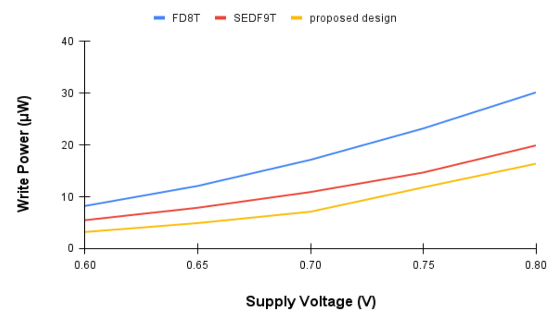

Fig. 5: Write power V_s supply voltage

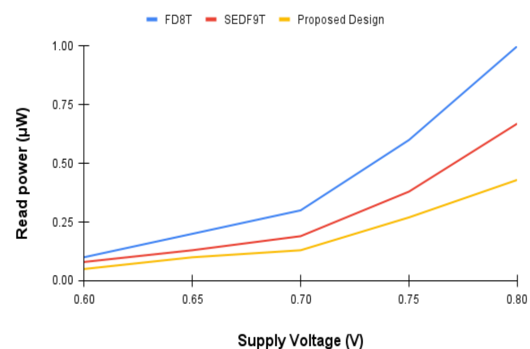

Fig. 6: Read power V_s supply voltage

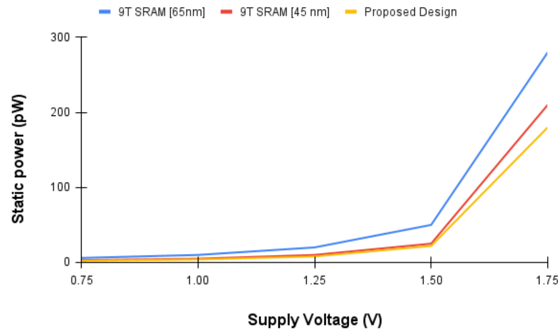

Fig. 7: Static power V_s supply voltage

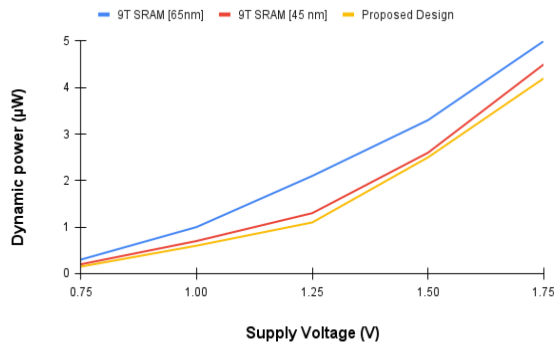

Fig. 8: Dynamic power V_s supply voltage

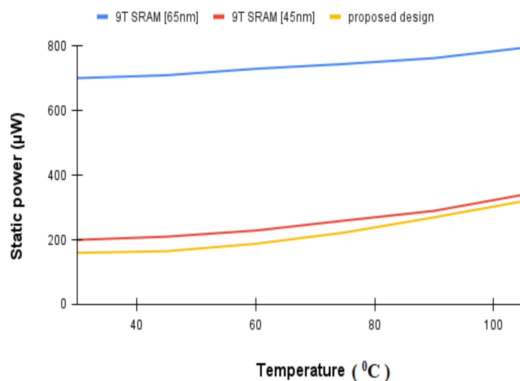

Fig. 9: Static power V_s temperature

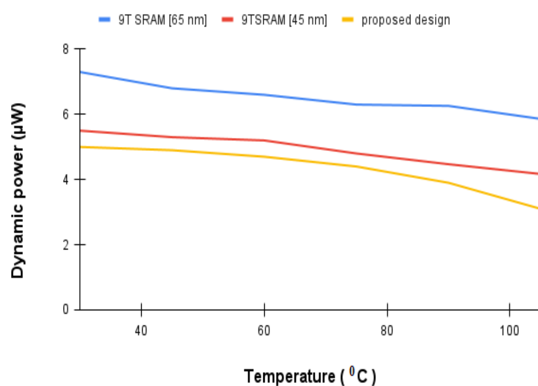

Fig. 10: Dynamic power V_s temperature

Static and Dynamic Power Versus Temperature

Power loss for dynamic and static performance with respect to temperature is discussed here. The dynamic energy used to switch the gate from one state to another was evaluated over a range of temperatures for different supply voltages. Here, Dynamic performance for all SRAM cells increases with temperature, while static power loss increases for both existing and proposed SRAM cells. From Fig. 9, it can be observed that the static power is increase linearly with the temperature and after 100°C it increases sharply. However, in Fig. 10, it can be seen that the dynamic power varies about the same for all SRAMs.

Data Retention Voltage (DRV)

DRV of SRAM shows minimum supply voltage at which it stores arbitrary state. As the supply voltage drops, it becomes more important to have "reliable" data. As a result, the DRV is the minimal voltage necessary to provide "stable" data and so preserve the cell's stability. DRV shows significant intra-chip variation in the deep submicron era. In our study, the DRV for 9T SRAM cells is 0.29 V; if this voltage is not met, data will flip from one state to another, resulting in undesirable output.

Conclusion

In this research, various SRAM cells are compared with the proposed 9T SRAM cell. The outcome of the proposed work shows the reduced energy on the sub-threshold regime has been studied. This article investigated the effect of several factors such as read, write, dynamic, static power against the supply voltage and temperature. When the supply voltage drops to the standby limit at 9T SRAM, the average memory capacity used can be significantly decreased by the cost of enlarging the cell space and the average reading capacity used. Also proposed 9T has a much better performance to other existing SRAM taken for comparison with reduced power consumption and data retention voltage for the circuit is 0.29 V, which is utilized to store the data in the circuit. All these improved result comes at a cost of reducing cell density. The future work of this proposed work is to design the circuit using the reversible logic gate for improving the leakage current.

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Author's Contributions

Pushkar Praveen: Worked on circuit design and analyzed the results. The author also worked in the text section of the presented work.

Rakesh Kumar Singh: Supervised the work with his expertise in the field of circuit designing for smart application.

Ethics

This study does not cover any such topic which requires ethical approvals and therefore not applicable. Regarding the ethics of journal submission guidelines are concerned that the paper has not been submitted elsewhere.

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